AMENDMENT TO THE CLAIMS

Please cancel claims 1-17. Please add the following new claims:

1-17 (Cancelled)

18. (New) A processing system comprising:

dispersal logic to receive a plurality of instructions;

an execution port coupled to said dispersal logic; and

a non-execution port coupled to said dispersal logic.

19. (New) The system of claim 18 wherein said non-execution port is to process instructions to take no action for an instruction cycle.

20. (New) The system of claim 19 wherein said execution port is to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

21. (New) A processing system comprising:

dispersal logic to receive a plurality of instructions;

a plurality of execution ports coupled to dispersal logic; and

a non-execution port coupled to said dispersal logic, said non-execution port to process instructions to take no action for an instruction cycle.

22. (New) The system of claim 21, wherein said plurality of instructions are taken from at least two individual threads.

23. (New) The system of claim 22 further comprising:

first and second instruction buffers coupled to said dispersal logic to store said plurality of instructions for first and second threads, respectively.

24. (New) The system of claim 23 wherein said plurality of instructions are grouped into bundles prior to processing in said non-execution and execution ports.

25. (New) The system of claim 22, wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

26. (New) The system of claim 21, wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

27. (New) The system of claim 26 wherein said plurality of instructions are grouped into bundles prior to processing in said non-execution and execution ports.

28. (New) A method of dispersing instructions in a multi-threaded processing system including a plurality of execution ports and at least one non-execution port, comprising:

determining if an instruction is an instruction to take no action for an instruction cycle; and

dispersing said instruction to take no action for an instruction cycle for execution by a non-execution port.

29. (New) The method of claim 28, wherein said plurality of instructions are taken from at least two individual threads.

30. (New) The method of claim 29 further comprising:

supplying said plurality of instructions to said dispersal logic from first and second instruction buffers coupled to dispersal logic to store said plurality of instructions for first and second threads, respectively.

31. (New) The method of claim 30, further comprising

processing instructions in said execution ports wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

32. (New) The method of claim 31 further comprising:

grouping said plurality of instructions into bundles prior to said supplying said instructions to said dispersal logic.

33. (New) The method of claim 28, further comprising:

processing instructions in said execution ports wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

34. (New) The method of claim 33 further comprising:

grouping said plurality of instructions into bundles prior to said supplying said instructions to said dispersal logic.